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L3	L2 and (tunnel adj oxide)	9	L3
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☐ 1. Document ID: US 6607925 B1

L4: Entry 1 of 1 File: USPT Aug 19, 2003

US-PAT-NO: 6607925
DOCUMENT-IDENTIFIER: US 6607925 B1
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TITLE: Hard mask removal process including isolation dielectric refill

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US-PAT-NO: 6607925
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TITLE: Hard mask removal process including isolation dielectric refill

DATE-ISSUED: August 19, 2003

INVENTOR-INFORMATION:

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US-CL-CURRENT: 438/4; 257/E21.279, 257/E21.546, 438/201, 438/257, 438/435

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L4: Entry 1 of 1 File: USPT Aug 19, 2003

DOCUMENT-IDENTIFIER: US 6607925 B1
** See image for Certificate of Correction **
TITLE: Hard mask removal process including isolation dielectric refill

Brief Summary Text (11):
According to the system and method disclosed herein, removing a majority of the hard mask using a wet etch, rather than removing all of the hard mask, prevents the wet etch from damaging the first material. And using a dry etch to remove the remainder of the hard mask substantially eliminates gouging.

Detailed Description Text (4):
FIG. 1 is a flow chart illustrating the fabrication steps used to pattern Poly 1 into floating gates using a hard mask. FIGS. 2A-2I are cross-sectional views of the silicon substrate during the fabrication steps described in FIG. 1. The process begins by depositing a layer of Poly 120 over a tunnel oxide 25 and silicon substrate 22 in step 100. As shown in FIG. 2A, the substrate 22 includes insulating regions of the tunnel oxide 25 and isolation dielectric 24, such as such as TEOS (tetraethyl orthosilicate) or HDP (high-density plasma). The isolation regions are formed in-between active areas where transistors will be located. The tunnel oxide 25 and the isolation dielectric 24 are deposited by conventional methods, and will therefore not be discussed in detail.

Detailed Description Text (7):
After the Poly 120 has been etched, the spacers 32 and nitride mask 28' need to be removed in step 118. Conventional methods for removing the spacers 32 and hard mask 26' include utilizing either a dry etch, or a wet etch. FIG. 3 is a cross-sectional view of the substrate 22 showing that if the spacers 32 and hard mask 26' are removed using a dry etch, then gouges 34 are typically formed in the isolation dielectric 24.

Detailed Description Text (9):
FIG. 4 is a flow chart illustrating the process of repairing the gouges 34 in the isolation dielectric 24 in accordance with a preferred embodiment of the present invention. After the hard mask 28' is stripped from the Poly 120, a layer of isolation dielectric 40, such as TEOS or HDP, is deposited over the substrate in step 200. FIG. 5A is a cross-sectional view of the substrate showing the isolation dielectric 40. In a preferred embodiment, the same type of isolation dielectric 40 used to originally fill the trenches is deposited over the substrate after the hard mask removal. Also a preferred embodiment, the layer of isolation dielectric 40 may be approximately 500 to 2000 angstroms in thickness.

CLAIMS:

5. The method of claim 3 further including step of performing the hard mask removal during fabrication of a flash memory array in which the hard mask has been patterned on top of a layer of polysilicon that is deposited over a silicon substrate that has trenches filled with the first isolation dielectric layer.

7. A method of removing a hard mask during a semiconductor process, the method comprising the steps of: (a) depositing a layer of polysilicon over a substrate that includes insulating regions filled with a first isolating dielectric layer; (b) patterning a hard mask over the layer of polysilicon; (c) forming spacers along the edges of the hard mask; (d) using the spacers and the hard mask to pattern the polysilicon; and (e) removing the spacers and hard mask, wherein the removal creates gouges in the first isolation dielectric layer; (f) depositing a second layer of isolation dielectric over the first material, wherein the second isolation dielectric layer fills the gouges in the first isolation dielectric layer; and (g) polishing the second layer of isolation dielectric to remove the second layer of isolation dielectric from the first material.

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